CLAIMS

1. Semiconductor structure, especially in a semiconductor detector, with

- a weakly doped semiconductor substrate (HK) of a first or second doping type,

- a highly doped drain region (D, D1) of a second doping type, located at a first surface of the semiconductor substrate (HK),

- a highly doped source region (S) of the second doping type, located at the first surface of the semiconductor substrate (HK),

- a channel (K) extending between the source region (S) and the drain region (D, D1),

- a doped inner gate region (IG) of the first doping type, located in the semiconductor substrate (HK), at least partially below the channel (K), and

- a clear contact (CL) for the removal of charge carriers from the inner gate region (IG),

characterized in that

the inner gate region (IG) in the semiconductor substrate (HK) extends at least partially up to the clear contact (CL).

2. Semiconductor structure according to Claim 1, characterized in that the clear contact (CL) is located on the drain side relative to the source region (S).

3. Semiconductor structure according to Claims 1 or 2, characterized in that the clear contact (CL) is located at least partially between the source region (S) and the drain region (D, D1).

4. Semiconductor structure according to any one of the preceding Claims, characterized in that a drain/clear region (DCG), that can be selectively activated as an auxiliary clear contact or as a drain, borders to the clear contact (CL) and to the drain region (D, D1) or is led near to the drain region (D, D1).

5. Semiconductor structure according to any one of the Claims 1 to 3, characterized in that a source/clear region (SCG), that can be selectively activated as an auxiliary clear contact or as a source, borders to the clear contact (CL) and to the source region (S) or is led near to the source region (S).

6. Semiconductor structure according to any one of the preceding Claims, characterized in that, in the semiconductor substrate (HK) below the clear contact (CL), a doped shield region (CSH) of the second doping type is located which electrically shields off the clear contact (CL).

7. Semiconductor structure according to any one of the preceding Claims, characterized in that the inner gate region (IG) in the semiconductor substrate (HK) extends from the source region (S) up to the drain region (D, D1).

8. Semiconductor structure according to any one of the Claims 1 to 6, characterized in that the inner gate region (IG) in the semiconductor substrate (HK) is located at least partially below the drain region (D, D1) and the clear contact (CL) and is spaced apart from the source region (S).

9. Semiconductor structure according to any one of the preceding Claims, characterized in that the channel (K) immediately borders on the clear contact (CL).

10. Semiconductor structure according to any one of the Claims 1 to 8, characterized in that the channel (K) is extends to the clear contact (CL) up to a pre-specified distance.

11. Semiconductor structure according to any one of the preceding Claims, characterized in that the drain region (D, D1) is divided up into several partial regions which are spaced apart from one another.

12. Semiconductor structure according to Claim 11, characterized in that a first partial region of the drain region (D, D1) is directly contacted, while a second partial region of the drain region (D, D1) is contacted by way of an inversion layer below the drain/clear region (DCG).

13. Semiconductor structure according to any one of the preceding Claims, characterized by a first line transfer (L2) for contacting the drain region (D, D1).

14. Semiconductor structure according to any one of the preceding Claims, characterized by a second line transfer (L1) for contacting the clear contact.

15. Semiconductor structure according to any one of the preceding Claims, characterized in that a closed and/or ring-shaped gate region (G) is envisaged for the control of the channel (K).

16. Semiconductor structure according to Claim 15, characterized in that the clear contact (CL) and/or the drain region (D, D1) and/or the drain/clear region (DCG) are located

within the gate region (G), while the source region (S) is located outside of the gate region (G).

17. Semiconductor structure according to Claim 15, characterized in that the clear contact (CL) and/or the drain region (D, D1) and/or the drain/clear region (DCG) are located outside of the gate region (G), while the source region (S) is located within the gate region (G).

18. Semiconductor structure according to any one of the Claims 15 to 17, characterized in that the drain/clear region (DCG) adjoins the entire periphery of the gate region (G).

19. Semiconductor structure according to any one of the Claims 15 to 18, characterized in that the gate region (G) borders only with a part of the periphery on the drain/clear region (DCG) and with the rest of the periphery on a doped region of the second doping type that is joined to the drain region (D, D1) and/or borders on the drain region (D, D1).

20. Semiconductor structure according to any one of the preceding Claims, characterized in that the clear contact (CL) is divided up into several parts.

21. Semiconductor structure according to any one of the preceding Claims, characterized in that a region (RK) of the second doping type is located at a second surface of the semiconductor substrate (HK) for the purpose of depleting the semiconductor substrate (HK).

22. Semiconductor structure according to any one of the preceding Claims, characterized in that the first doping type is n-doped, whereas the second doping type is p-doped.

23. Semiconductor structure according to any one of the Claims 1 to 21, characterized in that the first doping type is p-doped, whereas the second doping type is n-doped.

24. Semiconductor structure according to any one of the preceding Claims, characterized in that the semiconductor substrate (HK) is silicon.

25. Semiconductor structure according to any one of the preceding Claims, characterized in that the drain/clear region (DCG) is a MOS region.

26. Semiconductor structure according to any one of the preceding Claims, characterized by the formation as depletion type with additional channel implantation.

27. Semiconductor structure according to any one of the preceding Claims, characterized by the formation as enrichment type without additional channel implantation.

28. Semiconductor structure according to any one of the Claims 4 to 27, characterized in that the drain/clear region (DCG) or the source/clear region (SCG) has underneath a surface-near implantation (SD) of the second doping type.

29. Detector, in particular a drift detector, with a semiconductor structure according to any one of the preceding Claims.